IN THE SPECIFICATION

Kindly replace paragraphs 81 and 117 with the following corresponding replacement paragraphs (changes highlighted):

--[0081] The rated current density of the diode J_F is set, leaving a certain leeway, usually at one third the current density Jii which causes impact ionization such that avalanche breakdown is caused at the current density three times as high as the rated current density J_F. The breakdown voltage BV and the rated current density J_F are related with each other by the following equation:

$$BV = \text{~~5.3 x 10}^{13}\text{~~}\underline{1.06 \times 10^{14}} (N_D + 3J_F/q\, \nu_{sat})^{-0.75}\text{--}$$

--[0117] Now the method of manufacturing a semiconductor device according to according to a thirteenth embodiment of the invention will be described in connection with manufacture of the semiconductor device according to the twelfth embodiment. Figs. 27 through 35 are cross sectional views describing the method of manufacturing a semiconductor device according to the thirteenth embodiment of the invention. Referring at first to Fig. 27, an n-type impurity 102 such as As is introduced by ion implantation 101 at the dose amount of from 1 x 10^{11} to 5 x 10^{11} cm^{-2}, 100 Kev into the surface portion of an n^--type bulk wafer 49, the specific resistance thereof is 55 Ω-cm. For example, bulk wafer 49 is an FZ wafer manufactured by the floating zone method. Bulk wafer 49 will be a second n-type drift layer 4 later. Referring now to Fig. 28, an n-type buffer layer 3 doped more heavily than n^--type bulk wafer 49 is formed by heat treatment of more than 800°C. The n-type buffer layer 3 is 5 μm in thickness at this stage. Referring now to Fig. 29, a single crystal layer 48 containing phosphorus is grown epitaxially on n-type buffer layer 3. The specific resistance of epitaxially-grown single-crystal layer 48 is 55 Ω-cm. The epitaxially-grown single-crystal layer 48 is 60 μm in thickness. The epitaxially-grown single-crystal layer 48 will be a first n-type drift layer 2 later. Referring now to Fig. 30, the surface of epitaxially-grown single-crystal layer 48 is treated by mirror finish. A thermal oxide film is formed on epitaxially-grown single-crystal layer 48, and the thermal oxide film is patterned. Then, an anode layer 1 of around 5 μm in thickness is formed by ion implantation (boron 1 x 10^{13} cm^{-2}. Kev) and by subsequent thermal drive (1150°C, 3 hours). Referring now to

Fig. 31, an anode electrode 6 is formed by sputtering Al-Si, and by patterning the Al-Si film. Then, a not shown protection film such as a nitride film is formed. Referring now to Fig. 32, the back surface of the bulk wafer 49 is polished by back grinding 103 such that the laminate is around 120 μm in thickness. Referring now to Fig. 32, an n-type impurity 105 such as phosphorus is introduced into the back surface of the polished laminate by ion implantation 104. Referring now to Fig. 33, an n-type impurity 105 is introduced by ion implantation 104 to the polished back surface of the bulk wafer 49. Referring now to Fig. 34, an n-type cathode layer 5 is formed by annealing the implanted n-type impurity 105 at a low temperature, for example 400 °C, at which the Al-Si film is not deteriorated. The impurity concentration in n-type cathode layer 5 is 1×10^{17} cm^{-3} or higher. The diffusion depth of n-type cathode layer 5 is 0.5 μm. Referring now to Fig. 35, a cathode electrode 7 is formed on n-type cathode layer 5.--